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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,959	02/19/2004	Christophe Chevallier	400.184US02	4461

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EXAMINER	
MEMULA, SURESH	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,959	CHEVALLIER ET AL.	
	Examiner	Art Unit	
	Suresh Memula	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the amendments and remarks filed on 05/29/2007. The remarks are not persuasive; therefore, the rejections based on the prior art of record, Aji et al., are maintained. Claims 1-20 are pending.

Claim Objections

1. In claim 1, at line 6, the phrase "the marked line" lacks proper antecedent basis.

2. In claim 2, 8, 14 and 18, all at line 7, the phrase "the marked line" lacks proper antecedent basis.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-5, 8-11, 14-15, and 17 are rejected under 35 U.S.C. 102(b)** as being anticipated by US Patent No. 5,831,867 to Aji et al. (Aji).

5. As to claim 14, and similarly recited claims 1-2 and 8,

identifying with a line width marker any lines having a line width greater than a minimum line width {Column 7, lines 55-67; Column 8, lines 5-8; FIG. 5B; e.g. "wire data" is analogous to the claimed "line width marker"};

containing each line width marker in a line width layer {Column 7, lines 58-62; Although the prior art does not use the term "line width layer", the prior art does disclose the wire data, i.e., line width marker, is retrieved from the layout file (Column 7, lines 58-59), wherein the layout file includes layers (Column 6, lines 19-21), i.e., line width layer};

associating a line width parameter with each line width marker {Column 8, lines 5-11, 14-16; e.g. the minimum wire width, i.e., line width parameter, is associated with each wire width in the wire data, i.e., line width marker}, the line width parameter corresponding to a line width for the marked line {Column 8, lines 5-8; e.g., the minimum wire width, i.e., line width parameter, corresponds to a line width for the marked line};

comparing the line width parameter for each line width marker with an actual layout line width {Column 8, lines 5-8; e.g., decision 518 of FIG 5B decides whether the "wire width of the wire according to the integrated circuit design", i.e., actual layout line width, is greater than minimum wire width, i.e., line width parameter}; and

generating an error condition when the actual layout line width is less than the line width parameter (Column 8, line 8; FIG. 5B, element #520).

6. As to claim 3 and similarly recited claim 15, wherein a layout that contains the layout line further comprises a component layer having components of the integrated circuit (Column 6, lines 19-21).

7. As to claim 4 and similarly recited claim 9, and further comprising indicating an error when the actual layout line width is less than the line width parameter (Column 8, line 8; FIG. 5B, element #520).

8. As to claim 5 and similarly recited claim 10, further comprising recording an error when the actual layout line width is less than the line width parameter (Column 8, line 8; FIG. 5B, element #520).

9. As to claim 17, further comprising indicating or recording the error condition (Column 8, line 8; FIG. 5B, element #520).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 6, 12, and 18-19 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Aji in view of one or more of:

US Patent No. 6,117,179 to Tan et al. (Tan) and/or

US Patent No. 6,557,149 to Morrise et al. (Morrise).

12. Aji teaches substantially all of the limitations as stated above, except for excluding checking for errors above a transistor or in predetermined areas of the IC.

13. Tan discloses excluding checking for errors in areas near or above a transistor (Column 5, lines 11-17), and Morrise discloses excluding checking for errors in areas near or above a transistor (Column 15, lines 17-23).

14. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have excluded checking for errors in areas near or above a transistor; as taught by Tan (Column 5, lines 11-17) and/or Morrise (Column 15, lines 17-23); in order to ignore devices such as transistor (Tan: Column 5, lines 11-17), and/or ignore transistors for efficiency (Morrise: Column 15, lines 17-23).

15. Pursuant to claim 19, wherein a layout that contains the layout line further comprises a component layer having components of the integrated circuit (Aji: Column 6, lines 19-21).

16. **Claims 7, 13 and 16 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Aji in view of one or more of:

US Pub. No. 2004/0212402 to Chonan (Chonan),

US Pub. No. 2004/0013023 to Mori et al. (Mori), and/or

US Pub. No. 2003/0200509 to Takabayashi et al. (Takabayashi).

17. Aji teaches substantially all of the limitations as stated above, except for lines carrying power to transistors.

18. Chonan discloses lines carrying power to transistors (Paragraph 0027), Mori discloses lines carrying power to transistors (Paragraph 0011), and Takabayashi discloses lines carrying power to transistors (Paragraph 0063).

19. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized lines carrying power to transistors; as taught by Chonan (Paragraph 0027), Mori (Paragraph 0011), and/or Takabayashi (Paragraph 0063); in order to form a path there between (Chonan: Paragraph 0027), supply a power source (Mori: Paragraph 0011), and/or provide a conventional connection (Takabayashi: Paragraph 0063).

20. **Claim 20 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Aji in view of one or more of:

Tan and/or

Morrise in further view of one or more of:

Chonan,

Mori, and/or

Takabayashi.

21. Aji in view of Tan and/or Morrise teach substantially all of the limitations as stated above, except for lines carrying power to transistors.

22. Chonan discloses lines carrying power to transistors (Paragraph 0027), Mori discloses lines carrying power to transistors (Paragraph 0011), and Takabayashi discloses lines carrying power to transistors (Paragraph 0063).

23. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to have utilized lines carrying power to transistors; as taught by Chonan (Paragraph 0027), Mori (Paragraph 0011), and/or Takabayashi (Paragraph 0063); in order to form a path there between (Chonan: Paragraph 0027), supply a power source (Mori: Paragraph 0011), and/or provide a conventional connection (Takabayashi: Paragraph 0063).

Response to Applicant Remarks

24. The applicant states "....Aji et al. does not include each and every recitation of each of claims 1, 2, 8, and 14....".

Examiner's response:

25. **Regarding claims 1, 2, 8 and 14**: , Aji teaches the width of all wires is contained in the wire data (Column 7, lines 59-62), and the width of each wire is obtained from the wire data (Column 7, lines 59-62; FIG. 5B). The decision step (FIG. 5B, element #518) identifies (FIG. 5B, "YES") all lines greater than a minimum line width (Column 8, lines 4-7; FIG. 5B, element #518) by means of the wire data, i.e., with a line width marker. In view of the dictionary definition of "with", "wire data" itself is properly analogous to the claimed "line width marker" because (i) "wire data" is the agent that results in the identification of lines having a width greater than a minimum line width, and (ii) data itself can reasonably be interpreted as a "marker" for a line.

26. Aji teaches the wire data, i.e., line width marker, is retrieved from the layout file (Column 7, lines 58-59). Although the prior art does not use the term "line width layer", the prior art does disclose the wire data, i.e., line width marker, is retrieved from the layout file (Column 7, lines 58-59), wherein the layout file includes layers (Column 6, lines 19-21) and contains the wire data (Column 7, lines 58-59), i.e., line width layer.

27. Aji teaches a comparison step (Column 8, lines 5-8; FIG. 5B, element #518) determines if the wire width of the wire according to the IC design, i.e., actual layout line width/marked line, is greater than the associated minimum width of the wire (Column 8, lines 5-11; FIG. 5B, element #518), i.e., line width parameter.

28. Aji teaches generating an error condition if the wire width of the wire according to the IC design (Column 8, lines 5-11; FIG. 5B, elements #518, #520), i.e., actual layout line width/marked line, is not greater than the associated minimum width of the wire, line width parameter (Column 8, lines 5-11; FIG. 5B, elements #518, #520).

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suresh Memula
Art Unit 2825
August 16, 2007

JACK CHIANG
SUPERVISORY PATENT EXAMINER